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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,469	11/10/2003	Patrick J. Garavan	H0682.70002 US00	5727

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EXAMINER	
JAGAN, MIRELLYS	

ART UNIT	PAPER NUMBER
2859	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,469	GARAVAN, PATRICK J.	
	Examiner	Art Unit	
	Mirellys Jagan	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,20 and 21* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 19 is objected to because of the following informalities:

In claim 19, it is not clear how the first and second term of the ratio are 'coupled' to the first and second transistors since a ratio is not a physical object that can be coupled to transistors. Accordingly, the claim 19 not been further treated on the merits. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-11, 17, 18, 20, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,808,307 to Aslan et al [hereinafter Aslan].

Referring to claim 1, Aslan discloses a circuit adapted to provide at an output an output current defined by an average of ratios of measurement currents, each ratio provided by a plurality of equivalent current sources coupled in common to a current output, a first term of each ratio being defined by a selected one of the current sources and a second term of the ratio being defined by the remaining current sources, wherein the circuit is adapted to enable a selective changing of each of the current sources providing the first term until each of the current sources has provided the first term, the output current being equivalent to the average of the sum of ratios determined (see figure 1 and 3; column 2, lines 46-63; column 3, lines 1-24; column 4, lines 11-22 and 36-45; column 4, line 52-column 46; and column 7, lines 2-5).

Referring to claims 2-11, 17, 18, 20, and 22, Aslan discloses a chip having a circuit comprising:

a plurality of equivalent current sources (110) each being individually switchable to at least one transistor (120), the current sources being arranged to generate a PTAT voltage at the output of the transistor, the PTAT voltage being defined by an applied current coupled to the transistor and representing the temperature measured by the circuit;

a digitizer (114) adapted to digitize the voltage such that each of the values representative of the voltage is a digital 'word', i.e., is digital data;

storage circuitry (118) adapted to store a digital value representative of the generated voltage for each of the ratios;

averaging components (116) adapted to define an average digital value for the stored values representative of the voltage determined in each of the sequential coupling steps and a temperature of the chip; and

wherein the applied current is provided by a ratio of the current sources; a first term of the ratio is provided by a selected one of the current sources and a second term of the ratio is provided by the remaining current sources; the circuit is adapted to enable a selective changing of each of the current sources providing the first term of the ratio; and the circuit is adapted to enable shuffling through the current sources to change the selected one of the current sources providing the first term thereby sequentially coupling the currents, each defined by a ratio of the current sources, to the transistor; the circuit is adapted to shuffle the current sources so that each has provided the first term of the ratio; the number of current sources provided is 16; and the circuit can have two PN junctions, i.e., two transistors, such that the currents can be applied to each junction and a voltage proportional to absolute temperature can be obtained through sequential coupling of the transistors to either of the current sources or the remaining of the current sources, the voltages being subtracted from each other once obtained, i.e., the voltages are out of phase (not the same) (see figure 1 and 3; column 2, lines 46-63; column 3, lines 1-24; column 4, lines 11-22 and 36-45; column 4, line 52-column 46; and column 7, lines 2-5).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aslan in view of U.S. Patent 5,982,221 to Tuthill.

Aslan discloses a circuit having all of the limitations of claims 15 and 16, as stated above in paragraph 4, except for the transistor being a bipolar transistor or a parasitic transistor in a CMOS implementation.

Tuthill discloses a temperature measuring circuit having switched current sources for applying a current to a PN junction for measuring temperature. Tuthill teaches that useful alternate PN junctions for the temperature sensor are a transistor, a bipolar transistor, or a parasitic substrate bipolar transistor in a CMOS circuit (see column 2, lines 27-29).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit disclosed by Aslan by replacing the transistor with either a bipolar transistor or a parasitic transistor in CMOS circuit since Tuthill teaches that all of these transistors are useful alternative PN junctions for measuring temperature in a circuit.

7. Claims 12-14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aslan in view of U.S. Patent Application Publication 2001/0026576 to Beer et al [hereinafter Beer].

Aslan discloses a circuit having all of the limitations of claims 12-14 and 21, as stated above in paragraph 4, except for the chip having circuitry adapted to couple a voltage from each transistor to pins for providing external access to the chip such that the voltage is measurable at the pins to enable external calibration of the temperature sensed on the chip.

Beer discloses a chip having temperature-measuring circuitry for measuring temperature sensed by a PN junction. Beer teaches that useful to couple a voltage from PN junction to an exterior pin for providing external access to the chip such that the voltage is measurable at the pin to enable testing of the PN junctions on the chip (see paragraphs 4, 8, and 9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit disclosed by Aslan by coupling the voltage from each of the transistors of the chip to exterior pins for providing external access to the chip, as taught by Beer, in order to enable testing of the transistors.

Furthermore, the recitation that the pins are for enabling calibration of the temperature, externally evaluating the voltages, and providing a duel function in addition to the calibrating function are considered to be a recitation of the intended use of the pins and has not been given patentable weight since it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. See ***Ex parte Masham***, 2 USPQ2d 1647 (1987).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents disclose a temperature-sensing circuit:

U.S. Patent 6,008,685 to Kunst
U.S. Patent 6,097,239 to Miranda, Jr. et al
U.S. Patent 5,961,215 to Lee et al
U.S. Patent 6,554,469 to Thomson et al
U.S. Patent 6,078,208 to Nolan et al
U.S. Patent 6,674,185 to Mizuta

The following patents disclose a temperature-sensing circuit on a chip:

U.S. Patent 5,379,230 to Morikawa et al
U.S. Patent 6,169,442 to Meehan et al
U.S. Patent 4,165,642 to Lipp

The following patents disclose a current-producing circuit:

U.S. Patent 5,608,348 to Kearney et al
U.S. Patent 6,373,330 to Holloway
U.S. Patent 6,529,066 to Guenot et al
U.S. Patent 6,664,843 to Dasgupta et al

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mirellys Jagan whose telephone number is 571-272-2247. The examiner can normally be reached on Monday-Friday from 11AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MJ
December 7, 2004

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Supervisory Patent Examiner
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